High Temperature Electronics for Future Venus Exploration

A. H. Monica[1], D. M. Deglau[1], D. Maier[2], E. Kohn[2], N. R. Izenberg[1] and S. J. Papadakis[1]
[1]Johns Hopkins University Applied Physics Laboratory, 11100 Johns Hopkins Road, Laurel, MD, 20723, USA
[2]Institute of Electron Devices and Circuits, University of Ulm, Ulm, Germany

Poster #4032
Venus Lab and Technology Workshop (2015)
April 7-8
Hampton, VA

Introduction

- High temperature atmospheric environments are extremely difficult to measure in-situ. Up to now, large, massive, refrigerated spacecraft have been needed to conduct surface investigations of Venus, which has surface temperatures of 740 K. Autonomous in-situ exploration of the hotter temperatures (1000+ K) of volcanic vents has not been possible. The ability for mechanicals and instruments to comfortably function in these extreme temperature environments is essential to future Venus exploration efforts.
- Here we propose high-temperature capable microelectronics that are based upon arrays of carbon nanotubes (CNTs) which can operate in both high radiation and high temperature environments without requiring shielding or thermal management. Presently there is a clear need for such technology in order to enable future missions to explore Venus.

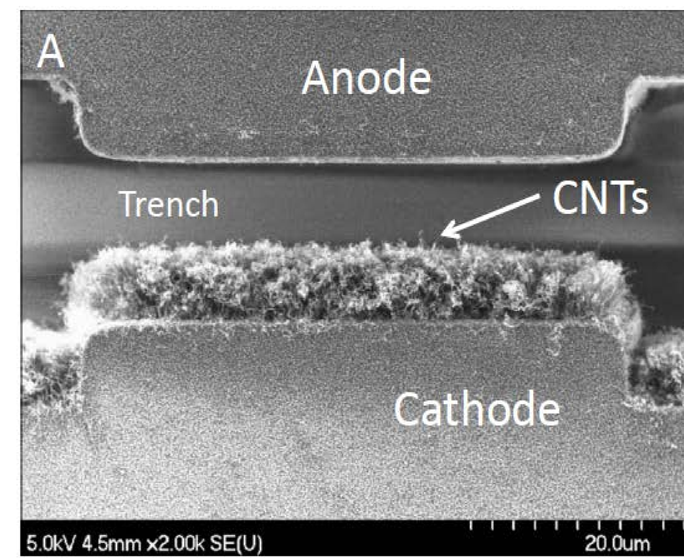


Figure 1: SEM image showing a top-down view of an array of CNTs selectively grown on the cathode of a device.

Approach

- Field emission based device
  - Emission → weak temperature dependence
  - Low power → no filament to heat
  - Radiation hard → no semiconductors; active region is vacuum
- Carbon nanotube electron emitters
  - Wide operating range (20K – 900K)
  - Redundancy: many emitters = device longevity
  - Large current carrying ability
- Fabrication
  - Robust materials: quartz, Ti, Ni, CNTs
  - Scalable and compatible with ICs

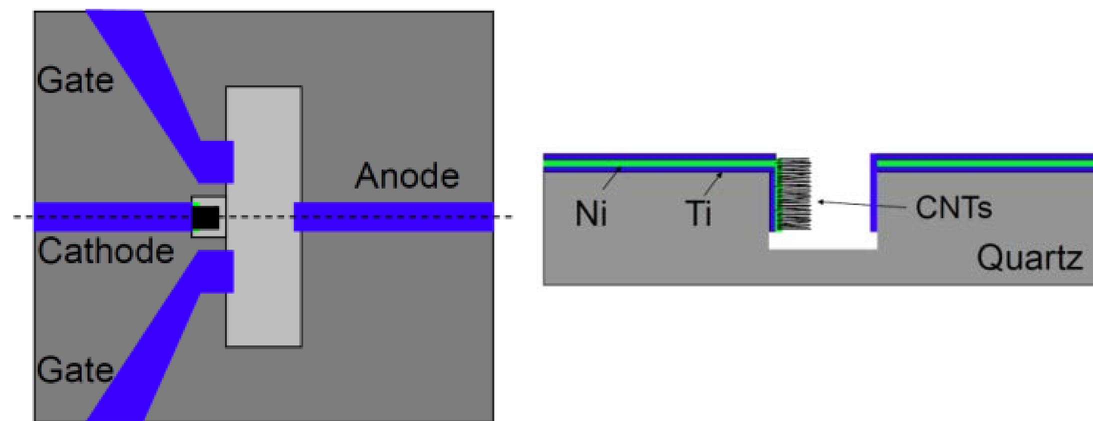
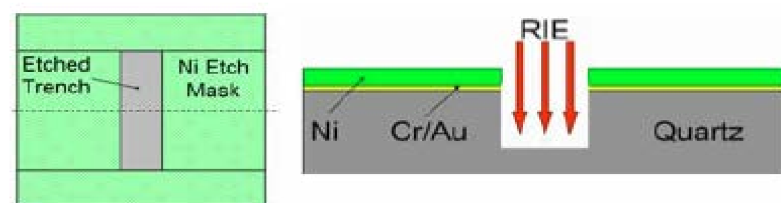


Figure 2: (Left) Cross section and (Right) top-down schematic of the CNT-based field emission device in a triode configuration. The entire device can be fabricated on a single substrate making it compatible with standard microelectronic processing methods.

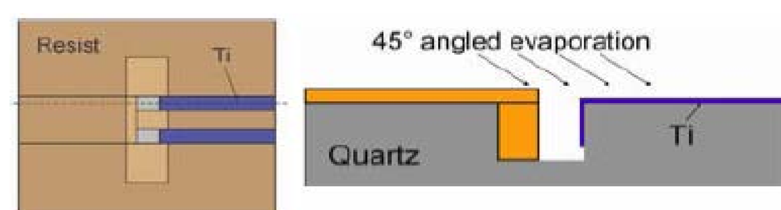
Fabrication

1. RIE Etch of Quartz Substrate



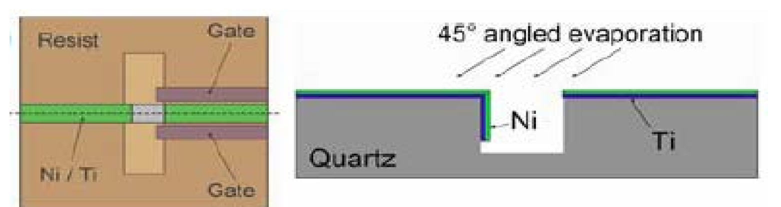
- Evaporation of 30 nm Cr and 200 nm Au on quartz substrate
- Optical lithography and wet etch to form vias in Cr/Au layer
- Electroplate ~3 µm Ni to form RIE etch mask
- RIE etch to form ~35 µm deep trenches; mask removal
- HF wet etch to smooth trench floor and sidewalls

2. Electrode Lithography + Gate Formation



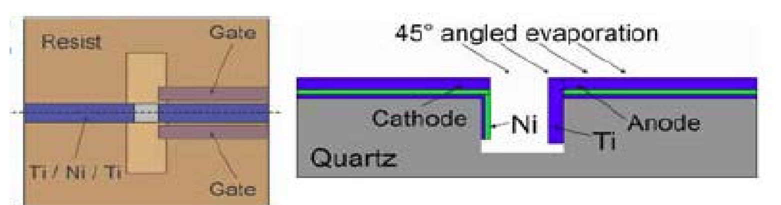
- Lithography to form gate electrode pattern
- Mount in evaporator at 45° to metal source
- Deposit 500 nm Ti; lift-off unwanted metal

4. Cathode Formation



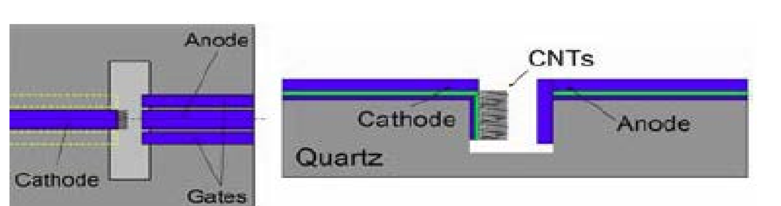
- Lithography to form anode / cathode pattern
- Deposit 100 nm Ti followed by 5 nm of Ni catalyst at 45° angle

5. Anode Formation



- Rotate substrate 180°; return to evaporator at 45° to metal source
- Deposit 700 nm Ti to form anode and cover Ni layer
- Lift-off unwanted metal in acetone

6. Thermal CVD CNT Growth



- Thermal CVD to only grow CNTs laterally from sidewall
- Ti layer prevents CNT growth from underlying Ni
- *Alternative gate locations shown in yellow*

Results and Discussion

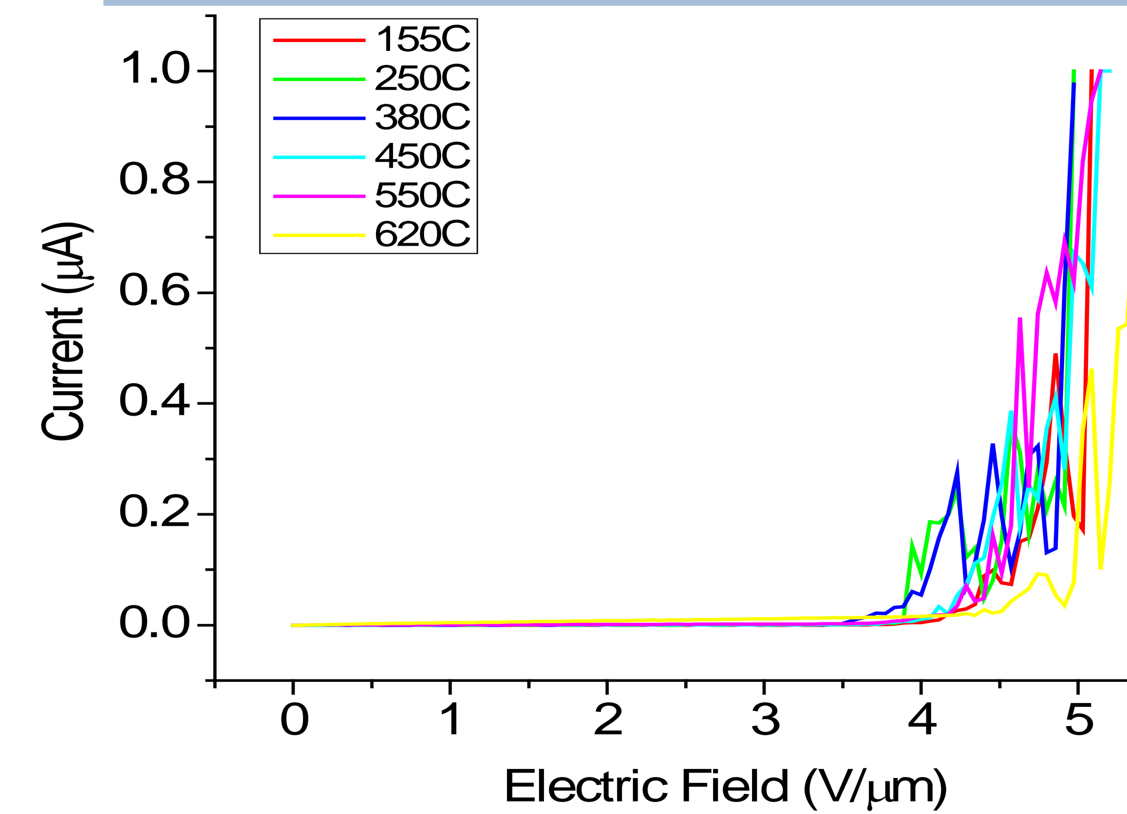


Figure 3: Diode Thermal/Electrical Results
- Anode-cathode spacing of 35 microns
- I-E characteristics measured in vacuum from RT to 620°C
- Turn on E-field of ~4.6 V/µm for 1 mA/cm² current density (A=5.0×10^{-6} cm²)

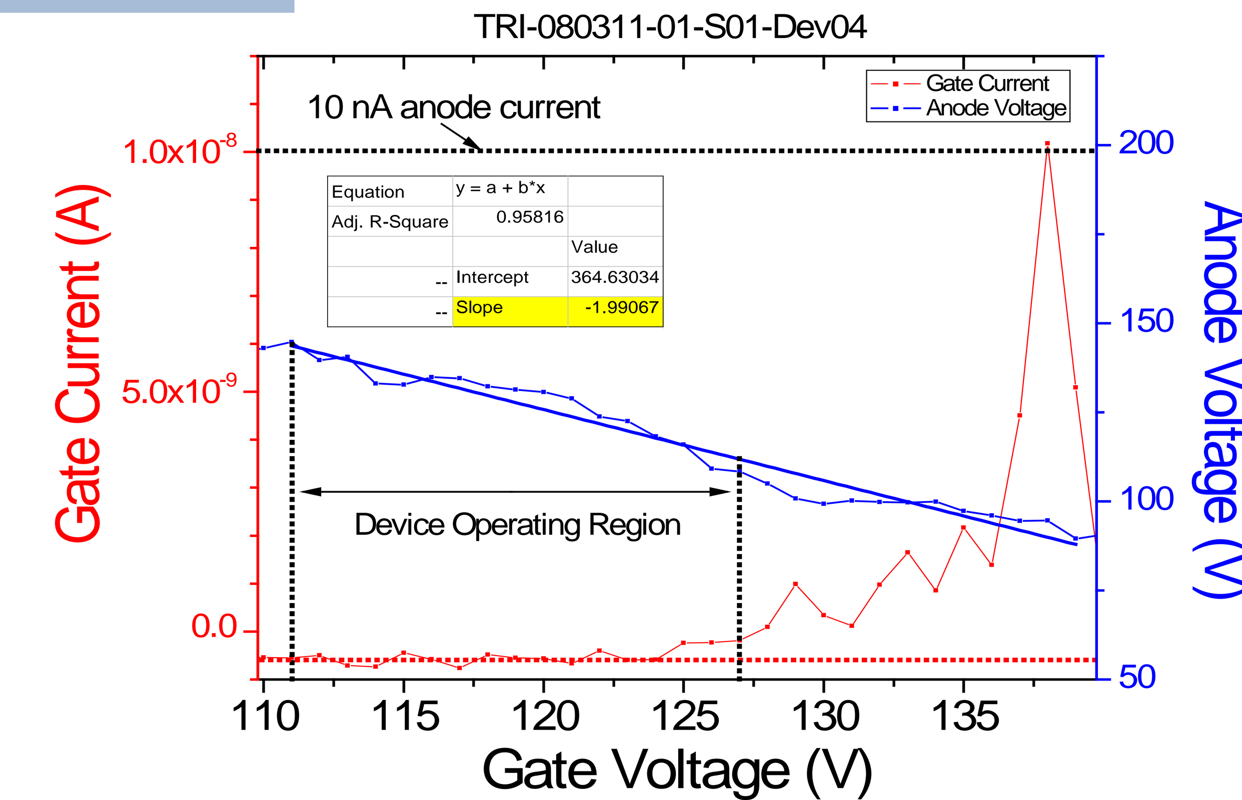
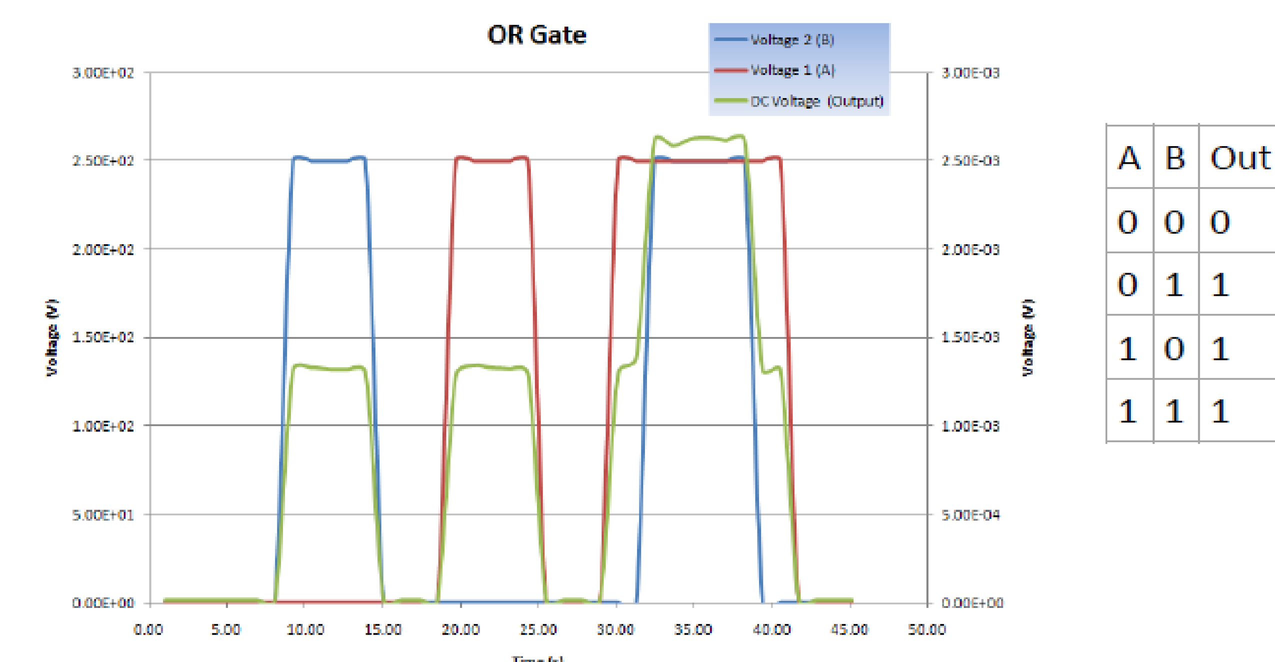


Figure 4: Triode Electrical Results
- Constant current of 10 nA applied between anode and cathode while measuring the anode voltage
- Gate voltage swept from 0 to 140V at RT in vacuum
- V_{anode} / V_{gate} = -2 → suggests effective gating
- "Operating Region" of device implies triode characteristics with very low leakage current
- Red dashed line is the zero-current offset of the SMU



A	B	Out
0	0	0
0	1	1
1	0	1
1	1	1

Figure 5: (Left) CNT diodes operating as an OR gate. Here, a 250V input signal was applied at A and/or B and the resulting output measured across a 1 kΩ resistor. For each input, a 250V signal corresponded to a digital "1" while a zero voltage represented a logical "0". On the output, a voltage of 1.25 mV (or higher) was considered a logical "1" and zero voltage was again a logical "0". The resulting truth table is shown and indicates appropriate OR gate behavior. This test was conducted in vacuum and the temperature was ramped from RT to 400°C without a change in operating characteristics.

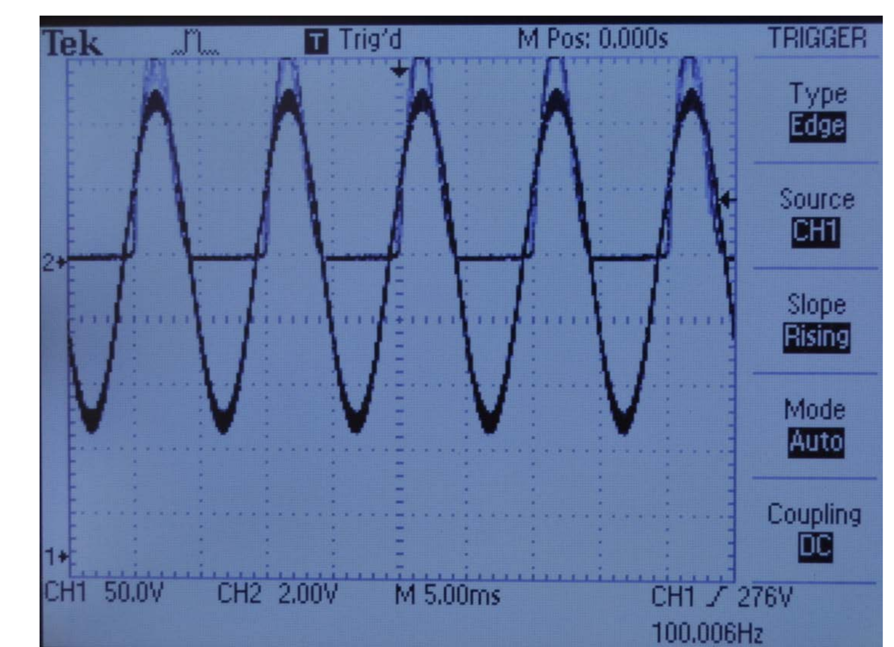


Figure 6: (Above) CNT diode operating as a half wave rectifier. Here, a 100 kHz input signal with a 250V peak-to-peak amplitude riding on a 250V DC offset was used. The DC offset is needed to ensure that the CNT diode would be just below it's turn-on voltage. This allows the 100 kHz, 250V peak-to-peak signal to cycle the diode. The output current from the rectifier was then sent to a current amplifier where it was amplified at 20 µA/V. The resulting voltage was then returned to the oscilloscope (light blue trace) to be displayed and compared to the input signal. These results indicate that the CNT diode half-wave rectifier functions properly.

Current Challenges

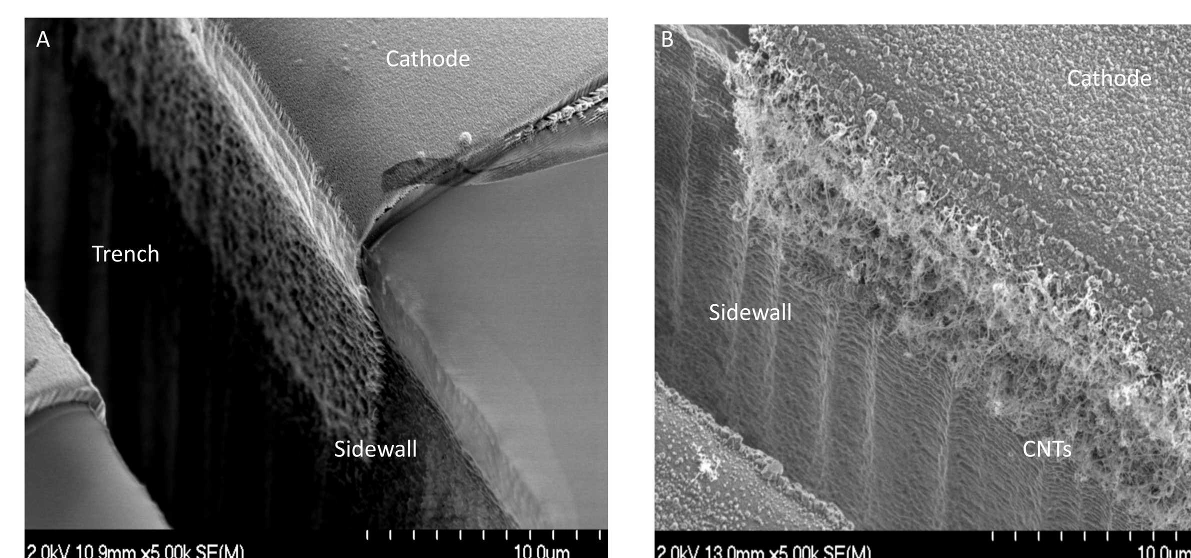


Figure 7: Current technical challenges
- Gate-to-anode shorting → caused by lithographic errors and CNT growth from exposed Ni catalyst a electrode edges
- Improving gate effectiveness → must be in close proximity to cathode without causing shorts or generating too much leakage current
- Metal continuity from top surface to trench sidewall → reduce trench width to facilitate easier lithography; thicken metal